Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

Claims 1-10. (Canceled)

11. (Currently amended) A communication system comprising a transmitter and a receiver,

the transmitter comprising a digital input, a coding device for generating data bits for transmission, and means for transmitting the data bits during respective frames of a transmission channel, the coding device comprising a coding circuit for generating a coded output having a greater number of bits than the digital input, an interleaving circuit for operating on the coded output to generate a data block comprising a plurality of interleaved words, and a rate matching circuit for adjusting the number of bits in the data block, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits, and means for selecting the rate matching pattern depending on an associated ~~a~~ bit ~~deletion/repetition rate, wherein a bit deletion/repetition~~ deletion or repetition pattern that is selected to ensure that the deleted or repeated bits of the data block are not required to enable all bits from the digital input to be reconstructed, and

the receiver comprising means for receiving the data bits and a data reconstruction circuit having means for adjusting the number of bits in the data block to reverse the action of the rate matching circuit, thereby reconstructing the interleaved words, a de-interleaving circuit having means for generating each of the plurality of interleaved words, and a channel decoder, the data

reconstruction circuit having means for selecting the rate matching pattern depending on the characteristics of the coding device.

12. (Currently amended) A system as claimed in claim 11, wherein said means for selecting select the rate matching pattern in such a way that all bits of the digital input can be derived from ~~the remainder of the~~ bits in ~~successive~~ the ~~interleaved~~ data block ~~blocks~~ other than the deleted or repeated bits of the data block.

13. (Currently amended) A system as claimed in claim 11, wherein the rate matching pattern for each interleaved word within the data block is offset with respect to the rate matching pattern of an ~~the~~ adjacent interleaved word or words within the data block.

14. (Currently amended) A system as claimed in claim 11, wherein said means for selecting select the rate matching pattern as a function of ~~the~~ an interleaving depth of the interleaving circuit.

15. (Currently amended) A system as claimed in claim 11, wherein the coding circuit applies convolutional coding and said means for selecting select the rate matching pattern as a function of a ~~the~~ constraint length of the convolutional code.

16. (Previously Presented) A system as claimed in claim 11, wherein the transmitter comprises additional coding devices, each for coding a respective digital input, and a multiplexer for combining output data words of said coding device and said additional coding devices for subsequent transmission by the transmission means on a single transmission channel.

17. (Previously Presented) A system as claimed in claim 16, wherein the outputs of said coding device and said additional coding devices are selected to have different data rates, the combined data rate corresponding to the channel capacity of the transmission channel.

18. (Currently Amended) A system as claimed in claim 11, wherein the rate matching pattern forms a matrix including change bits that indicate a change of corresponding bits of said interleaved words within said data block, wherein each row of said matrix includes a maximum of one of said change bits.

19. (Currently Amended) A system as claimed in claim 11, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source.

20. (Previously Presented) A system as claimed in claim 11, wherein said interleaving circuit is not adaptive.

21. (Currently Amended) A system as claimed in claim 11, wherein said interleaving circuit has a constant input bit rate.

22. (Currently Amended) A system as claimed in claim 11, wherein said coding circuit has one of: (a) a fixed code rate and (b) a predetermined number of rates for a variable data source, and wherein said interleaving circuit is not adaptive.

23. (Currently amended) A system as claimed in claim 11, wherein said rate matching circuit alters a coding rate of said coding circuit according to the bit deletion or repetition pattern.

24. (Currently amended) A method of operating a communication system comprising a transmitter and a receiver, the method comprising:

the transmitter operating on the digital input to generate a coded output having a greater number of bits than the digital input, operating on the coded output to generate a data block comprising a plurality of interleaved words and adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, and

the receiver receiving the data bits, adjusting the number of bits in the data block to reverse the action of the rate matching operation, thereby reconstructing the interleaved words, and de-interleaving and decoding the interleaved words to reverse the actions of the interleaving and coding operations, wherein the rate matching pattern is selected depending on an associated ~~a bit deletion/repetition rate, wherein a~~ bit ~~deletion/repetition~~ deletion or repetition pattern that is selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

25. (New) A system as claimed in claim 11, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.

26. (New) The method of claim 24, wherein said rate matching pattern includes change bits for deleting or repeating bits of said data block and said change bits are offset with respect to each other along adjacent columns of a matrix of said rate matching pattern.